

Rinzai Bell

Managing Engineer 2005

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Qualifications

Twenty years of hardware and firmware design experience ranging from precision analog and mixed signal instrumentation (NIM, VXI, VME and bench-top) to system design and implementation for a IS-136 Cellular Base Station. Schematic capture, PCB layout, FPGA/CPLD/PLD design, low level code (C, Pascal, assembly). Familiar with OrCad, PwerPCB (PADS), Actel, AMD (now Lattice) MACH1-5, Altera, Cypress CPLD, VHDL, C, 8051/x86/MIPS/68xx Assembly.

Experience with taking an idea from product conception through prototypes, and into manufacturing with a strong emphasis on DFM & DFT.

Experience

Andros, Inc., Richmond, California (March 1998 – Present)

Manager of Research and Development (Electrical)

Senior Electronics Engineer:

- Responsible for the management of several mid-level engineers and technicians.
- Implemented two generations of Non Dispersive Infrared Spectroscopy based gas analyzers for automotive and medical applications.
- Designed a third generation of Dispersive Infrared Spectroscopy analyzer for medical anesthetic applications.
- Responsible for realizing UL certification for electrical emissions, susceptibility, and safety.
- Cost reduced, and redesigned numerous products for in-circuit testing and manufacturability.
- Managed the retooling of all of the test & measurement equipment and redesign the computer infrastructure, after a fire in 2000 destroyed nearly all of the company.

Aval Communications, Inc., Walnut Creek, California (March 1996 - March 1998)

Senior Electronics Engineer:

- Managed mid-level engineers and technicians.
- Responsible for implementation of an IS-136 wireless base station.
- Designed an overall system consisting of a dual single board computer (“SBC”), 16 Modulator-Demodulators (“Modems”), 8 Voice Encoders (“Vocoders”), and 2 Network Interface Cards (“NIC”) (E1/T1), dual master oscillators, and power supplies. The system supported “hot insertion” and redundant SBCs, NICs and master oscillators.
- Designed and implemented subsystems which consisted of the Modem, utilizing the Analog Devices ADSP2181 DSP; the NIC utilizing an AM80186 uP; and the back-plane which supported the 16 radios, 8 Vocoder, Redundant Processors / NIC / Oscillator / Power supply.

Senior Electronics Engineer (Continued)

- Ported over two ROM analysis kernels (one for the R3000, another for the AM186). This involved writing assembly and C code.
- Wrote the VxWorks Board Support Packages for an IDT supplied evaluation card as well as our SBC.
- Designed and implemented second generation SBC utilizing IDTs highly integrated R3000 based 79R36100. This is a “micro-base station” that consisted of a single controller and support for 4 modems. In the support of this project, I ported the Wind River Systems OS (BSP) to the target.

Highland Technology Inc., San Francisco, California (June 1994 - February 1996)

Hardware Design Engineer

- Presented a proposal to design a RADAR target simulator for a large defense contractor for which I was by hired by Highland to design and oversee. The simulator consisted of a VXI backplane, a 486 based SBC running LINX real time UNIX that would control a set of three VXI based Digital Delay Generators.
- Designed the VXI based Digital delay Generator (*DDG*). The DDGs utilized Actel FPGAs, ECL, TTL, + high-speed analog. This unit supported four-channels of programmable delay, settable to 20 ps, 83 ms full scale, 1ppm accuracy, and 100 ps of jitter with programmable output levels.
- Managed the SW engineer writing the application software that simulated targets using the above-described system.
- Proposed to Lawrence Livermore National Labs a VME version of the DDG, which was accepted for use in their National Ignition Facility used to simulate nuclear fusion reactions.
- Designed this second generation DDG, the V851, in VME format (6U) with six channels of delay where the jitter was reduced to 25 ps.

Berkeley Nucleonics Corporation, San Rafael, California (May 1984 - May 1994)

Hardware Design Engineer

- Key member of the design team for a bench-top pulse generator that supported a family of modular outputs. This generator consisted of a uP controller, a DDG, front panel interface and remote GPIB & RS232 ports.
- Designed Light Pulse Generator (LPG), high voltage (1000 Volt), and high speed GaAs based (100 ps transition) outputs modules for use in the 6040 platform.
- Assisted with writing of the software utilizing C and assembly language.
- Key team member in the design and implementation of non-CPU based bench top Light Pulse Generators.
- Responsible for management of 6 technicians in the test department.
- Wrote and implemented test and calibration routines (both manual & automated).

References available upon request.